AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A power supply system comprising:

~~a propagation delay detector that measures a propagation delay of a launch signal, and outputs a plurality of detection signals that identify the propagation delay; and~~

~~a latch circuit that latches the detection signals as a plurality of latched signals in response to a sample signal~~

a detector that measures a propagation delay of a signal edge, and outputs information that identifies the propagation delay of the signal edge; and

a voltage generator connected to the detector and a power node, the voltage generator having a number of resistive nodes, a number of resistive elements, and a number of switches, the resistive elements being connected in series such that each resistive element is connected between two resistive nodes, a first resistive element in the series being connected to a voltage source via a resistive node, a last resistive element in the series being connected to ground via a resistive node, each switch being connected to a resistive node and the power node.

2. (Currently Amended) The power supply system of claim 1 ~~and further comprising a digital to analog converter (DAC) connected to the latch, the DAC receiving the plurality of latched signals, and generating a voltage on a power node in response to the plurality of latched signals~~ wherein the voltage generator includes a controller that processes the information to output a number of control signals to the switches, the control signals turning on a switch to place a supply voltage on the power node.

3. (Currently Amended) The power supply system of claim 2 wherein the ~~DAC~~ controller includes[[:]] a decoder that converts the ~~plurality of latched signals to a plurality of edge words;~~ information into an edge word that has a series of bits, only one bit of the series of bits having a first logic state, each remaining bit of the series of bits having a second logic state

~~an integrator that averages a number of edge words to generate a plurality of control signals;~~

~~a plurality of control circuits connected to the power node, each control circuit receiving a control signal;~~

~~a plurality of resistor nodes, each resistor node being connected to a control circuit; and~~

~~a plurality of resistors connected to the plurality of resistor nodes such that each resistor is connected to a resistor node~~.

4. (Original) The power supply system of claim 3 wherein the decoder includes an exclusive OR gate.

5. (Original) The power supply system of claim 4 wherein the exclusive OR gate is free of a transmission gate.

6. (Currently Amended) The power supply system of claim 2 wherein the ~~plurality of~~ resistive elements are resistors ~~are connected in series~~.

7. (Currently Amended) The power supply system of claim ~~6 wherein the resistors are connected between a power supply voltage and ground~~ 3 wherein only one control signal has a first logic state, and each remaining control signal has a second logic state.

8. (Currently Amended) ~~The power supply of claim 2 wherein~~ A power supply system comprising:

a propagation delay detector that measures a propagation delay of a launch signal, and outputs a plurality of detection signals that identify the propagation delay, the propagation delay detector ~~includes~~ including a plurality of substantially equal delay blocks that have a corresponding plurality of outputs that output the plurality of detection signals as a thermometer code;

a latch circuit that latches the detection signals as a plurality of latched signals in response to a sample signal; and

a digital-to-analog converter (DAC) connected to the latch, the DAC receiving the plurality of latched signals, and generating a voltage on a power node in response to the plurality of latched signals.

9. (Currently Amended) The power supply of claim [[2]] 8 wherein the sample signal is a quadrature signal with respect to the launch signal, and the launch signal is a clock signal.

10. (Currently Amended) ~~The power supply system of claim 2 and further comprising~~ A power supply system comprising:

a propagation delay detector that measures a propagation delay of a launch signal, and outputs a plurality of detection signals that identify the propagation delay;

a latch circuit that latches the detection signals as a plurality of latched signals in response to a sample signal;

a digital-to-analog converter (DAC) connected to the latch, the DAC receiving the plurality of latched signals, and generating a voltage on a power node in response to the plurality of latched signals; and

a reset circuit that generates a reset signal in response to the launch signal and the sample signal, the reset signal resetting the propagation delay detector.

11. (Original) The power supply system of claim 10 wherein a rising edge of the sample signal precedes a rising edge of the launch signal.

12. (Original) The power supply of claim 10 wherein the power node is connected to the latch circuit and the reset circuit.

13. (Currently Amended) The power supply of claim 8 ~~wherein the plurality of delay blocks and the plurality of detection signals are unequal~~ and further comprising delay blocks that do not output a detection signal which are connected in series with the plurality of delay blocks.

14. (Currently Amended) The power supply system of claim 2 and further comprising a current boosting stage connected to the ~~DAC~~ power node.

15. (Currently Amended) The power supply system of claim [[9]] 8 wherein the latch circuit outputs the plurality of latched signals as a thermometer code.

16. (Currently Amended) A power supply system comprising:

a ~~plurality of~~ two or more power supply circuits, each power supply circuit having:

a propagation delay detector that measures a propagation delay of a launch signal, and outputs a plurality of detection signals that identify the propagation delay;

a latch circuit that latches the detection signals as a plurality of latched signals in response to a sample signal; and

a digital-to-analog converter (DAC) connected to the latch, the DAC receiving the plurality of latched signals, and generating a voltage on a power node in response to the plurality of latched signals; and

a ~~plurality of~~ two or more current boosting stages, each power supply circuit being connected to a current boosting stage.

17. (Currently Amended) The power supply system of claim 16 wherein the ~~plurality of~~ power supply circuits are formed on a first chip, and the ~~plurality of~~ current boosting stages are formed on a second chip.

18. (Original) The power supply system of claim 17 wherein the current boosting stages are operational amplifiers.

19. (Currently Amended) A method of providing power, the method comprising ~~the steps of~~:

~~measuring a propagation delay of a launch signal with a propagation delay detector, and outputting a plurality of detection signals that identify the propagation delay;~~

~~latching the detection signals in response to a sample signal to form a plurality of latched signals; and~~

~~generating a voltage in response to the plurality of latched signals, and outputting the voltage to the propagation delay detector~~

measuring a propagation delay of a signal edge, and outputting information that identifies the propagation delay of the signal edge;

simultaneously generating two or more substantially constant supply voltages from a voltage source; and

processing the information to place one of the supply voltages on a power node.

20. (Currently Amended) The method of claim 19 wherein ~~the sample signal is a quadrature signal with respect to the launch signal~~ processing includes converting the information into an edge word that has a series of bits, only one bit of the series of bits having a first logic state, each remaining bit of the series of bits having a second logic state.

21. (Currently Amended) The method of claim ~~19 wherein the generating step includes the step of converting the plurality of latched signals to a plurality of control signals, the control signals having first logic states and second logic states, and only one of the control signals having a first logic state at a time~~ 20 wherein the information that identifies the propagation delay of the signal edge is output as a thermometer code.

22. (New) The method of claim 21 wherein a group of edge words are averaged to determine which one of the supply voltages is placed on the power node.

23. (New) The power supply system of claim 3 wherein the information that identifies the propagation delay of the signal edge is output as a thermometer code.

24. (New) The method of claim 23 wherein a group of edge words are averaged to generate the control signals.